Substitute for Form 1449A/PTO (Modified)	Attorney Docket No.: 42390.P9429	Application Number: 09/608,637
Sheet 1 of 4	First Named Inventor: Jin Yang	Examiner: Unassigned IDS #4
	Filing Date: June 30, 2000	Art Unit: 2763

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (If known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EG		5,469,367		Puri et al	11-21-1995	
		5,491,639		Filkorn	02-13-1996	
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		5,754,454		Pixley et al	05-19-1998	
		5,768,498		Boigelot, et al	06-16-1998	
		5,905,977		Goubault	05-18-1999	
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		6,026,222		Gupta et al	02-15-2000	
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		6,247,165		Wohl et al	06-12-2001	
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		6,308,299		Burch et al	10-23- 2001	
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EG		6,339,837		Li	01-15-2002	

Examiner Signature	EDGARCIA-OTERO	Date Considered	2/29/04

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	Filing Date: June 30, 2000	Art Unit: 2763

OTHER ART – NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation[2]
A EG		BEREZIN, S. et al, "A Compositional Proof System for the Modal μ-Calculus and CCS," *Technical Report CMU-CS-97-105, Carnegie Mellon University,* January 15, 1997	
B EG		BEREZIN, S. et al, "Model Checking Algorithms for the μ-Calculus," *Technical Report CMU-CS-96-180, Carnegie Mellon University,* September 23, 1996	
C EG		BRYANT, R. E. et al, "Formal Hardware Verification by Symbolic Ternary Trajectory Evaluation," *28th ACM/IEEE Design Automation Conference,* Paper 24.2, 1991, pages 397-402	
D EG		BRYANT, R. E., "Binary Decision Diagrams & Beyond," Tutorial at ICCAD '95, *Carnegie Mellon University,* 1995	
E EG		BURCH, J. R. et al, "Representing Circuits More Efficiently in Symbolic Model Checking," *28th ACM/IEEE Design Automation Conference,* Paper 24.3, 1991, pages 403-407	
F EG		BURCH, J. R. et al, "Sequential Circuit Verification Using Symbolic Model Checking," *27th ACM/IEEE Design Automation Conference,* Paper 3.2, 1990, pages 46-51	
G EG		CAMPOS, S., "Real-Time Symbolic Model Checking for Discrete Time Models," *Technical Report CMU-CS-94-146, Carnegie Mellon University, Pittsburgh, PA,* May 2, 1994	
H EG		CHAN, W. et al, "Combining Constraint Solving and Symbolic Model Checking for a Class of Systems with Non-linear Constraints, *Computer Aided Verification, 9th International Conference, CAV '97 Proceedings (O. Grumberg, Editor),* Lecture Notes in Computer Science 1254, pages 316-327, Haifa, Israel, June 1997. Springer-Verlag (Revised in December '98)	
I EG		CHEN, Y. et al, "PBHD: An Efficient Graph Representation for Floating Point Circuit Verification," *Technical Report CMU-CS-97-134, Carnegie Mellon University,* May 1997	
J EG		CHEUNG, S. et al, "Checking Safety Properties Using Compositional Reachability Analysis," *ACM Transactions on Software Engineering and Methodology,* Vol. 8, No. 1, January 1999, pages 49-78	
K EG		CHIODO, M. et al, "Automatic Compositional Minimization in CTL Model Checking," *Proceedings of 1992 IEEE/ACM International Conference on Computer-Aided Design,* November, 1992, pages 172-178	

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OTHER ART – NO PATENT LITERATURE DOCUMENTS

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L EG		CHOU, C., "The Mathematical Foundation of Symbolic Trajectory Evaluation," *International Conference on Computer-Aided Verification(CAV'99)*, Trento, Italy, July 1999 pp. 196-207, Proceedings of CAV'99, Lecture Notes in Computer Science #1633 (Editors: Nicolas Halbwachs & Doron Peled), Springer-Verlog, 1999	
M EG		CLARKE, E. et al, "Another Look at LTL Model Checking," *Technical Report CMU-CS-94-114, Carnegie Mellon University,* February 23, 1994	
N EG		CLARKE, E. et al, "Combining Symbolic Computation and Theorem Proving: Some Problems of Ramanujan," *Technical Report CMU-CS-94-103, Carnegie Mellon University,* January 1994	
O EG		CLARKE, E. M. et al, "Formal Methods: State of the Art and Future Directions," *ACM Computing Surveys*, Vol. 28, No. 4, December 1996, pages 626-643	
P EG		CLARKE, E. M. et al, "Model Checking and Abstraction," *Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages,"* February 1992, pages 343-354	
Q EG		CLARKE, E. M. et al, "Model Checking and Abstraction," *ACM Transactions on Programming Languages and Systems,* Vol. 16, No. 5, September 1994, pages 1512-1542	
R EG		GRUMBERG, O., "Model Checking and Modular Verification," *ACM Transactions On Programming Languages and Systems*, Vol. 16, No. 3, May 1994, pages 843-871	
S EG		JACKSON, D., "Exploiting Symmetry in the Model Checking of Relational Specifications," *Technical Report CMU-CS 94-219, Carnegie Mellon University,* December 1994	
T T		JAIN, A. et al, "Verifying Nondeterministic Implementations of Determinist Systems," *Lecture Notes in Computer Science, Formal Methods in Computer Aided-Design*, pp. 109-125, November 1996	

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U EG		JAIN, A., "Formal Hardware Verification by Symbolic Trajectory Evaluation," *Carnegie Mellon University Ph.D. Dissertation,* July 1997	
V EG		JAIN, S. et al, "Automatic Clock Abstraction from Sequential Circuits," *Proceedings of the 32nd ACM/IEEE Conference on Design Automation,* January 1995	
W EG		JHA, S. et al, "Equivalence Checking Using Abstract BBDs," *Technical Report CMU-CS-96-187, Carnegie Mellon University, Pittsburgh, PA,* October 29, 1996	
X EG		KERN, C. et al, "Formal Verification In Hardware Design: A Survey," *ACM Transactions on Design Automation of Electronic Systems,* Vol. 4, No. 2, April 1999, pages 123-193	
Y EG		KURSHAN, R. et al, "Verifying Hardware in its Software Context," *Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages,* February 1992, pages 742-749	
Z EG		NELSON, K. L. et al, "Formal Verification of a Superscalar Execution Unit," *34th Design Automation Conference,* June 1997	
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AB EG		VELEV, M. N., "Efficient Modeling of Memory Arrays in Symbolic Simulations," *Proceedings of Computer-Aided Verification,* June 1997	
AC EG		WING, J. M. et al, "A Case Study in Model Checking Software Systems," *Technical Report CMU-CS-96-124, Carnegie Mellon University, Pittsburgh, PA,* April 1996	
AD EG		YEH, W. et al, "Compositional Reachability Analysis Using Process Algebra," *28th ACM/IEEE Design Automation Conference,* 1991	

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Sheet 1 of 1	First Named Inventor: Jin Yang	Examiner Unassigned IDS #5
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U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No.[1]	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (If known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EG		5,119,318	395/61	Paradies et al.	06/02/1992	
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